IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT:	Hyong-Gon Lee	EXAMINER: Abbas I. Abdulselam
SERIAL NO.:	09/934,590	GROUP ART UNIT: 2677
FILED:	August 23, 2001	Docket: 8071-131T (OPP010032US)
FOR:	LOW POWER LCD	

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Dated: March 28, 2006

Richard D. Ratchford, Jr.

PATENT APPLICATION

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Examiner: Abbas I. Abdulselam

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Group: Art Unit 2677

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APPEAL BRIEF

Appeal from Group 2677

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I. INTRODUCTION

This Appeal is from a Final Office Action mailed on June 28, 2005 (Paper No. 10) (hereinafter, referred to as the "Final Action") finally rejecting claims 1, 2, 4-8 and 11-18 of the above-identified application, and an Advisory Action mailed on October 18, 2005 (Paper No. 14). Applicants commenced this Appeal by a Notice of Appeal dated November 28, 2005, and hereby submit this Appeal Brief.

II. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is Samsung Electronics, Co. Ltd., the assignee of the entire right, title and interest in and to the subject application by virtue of an assignment recorded in the U.S. Patent and Trademark Office at reel 012111 frame 0412.

III. RELATED APPEALS AND INTERFERENCES

There are no Appeals or Interferences known to Applicants, Applicants' representatives or the Assignee, which would directly affect or be indirectly affected by or have a bearing on the Board's decision in the pending Appeal.

IV. STATUS OF CLAIMS

Claims 1-18 are pending and are under appeal. Claims 1, 2, 4-8 and 11-18 have been rejected. Claims 3, 9 and 10 have been indicated by the Examiner as being allowable if rewritten in independent form including all the limitations of their base claims and any intervening claims. The claims on appeal are set forth in the attached Appendix.

Claims 1, 5, 12, 16 and 18 are independent claims. Claims 2-4 directly depend from claim 1, claims 6, 10 and 11 directly depend from claim 5 and claims 7-9, 14 and 15 indirectly depend from claim 5, claim 13 directly depends from claim 12 and claim 17 directly depends from claim 16.

V. STATUS OF AMENDMENTS

Claims 1-11 and 13 were amended and claims 14-18 were added by the Amendment under 37 C.F.R. § 1.111, filed May 16, 2003. This Amendment was entered.

Claims 2, 4, 5, 8 and 12-16 were amended by the Amendment under 37 C.F.R. § 1.111, filed April 28, 2004. This Amendment was entered.

A Response to the Non-Final Office Action was mailed on February 22, 2005. The Response included no amendments. This Response was entered.

Claim 1 was amended by the Amendment under 37 C.F.R. § 1.116, filed September 28, 2005. This amendment was not entered.

VI. SUMMARY OF THE CLAIMED SUBJECT MATTER

In general, the claimed subject matter relates to a liquid crystal display (LCD) and an LCD panel driving method. The LCD includes a scan signal line, a source signal line, a pixel switch for outputting image signals, a power unit for supplying first power and second power to all pixels from outside of a pixel area of an LCD panel, a control signal line unit including a first control signal line for transmitting a first control signal to all pixels from outside of the pixel area and a second control signal line for transmitting a second control signal to all pixels from outside of the pixel area, a

liquid crystal (LC) unit for [transmitting light] according to a voltage difference between the image signals and the second power and a memory cell unit for receiving the first and second control signals.

A. Embodiment Of Claim 1

Claim 1 recites, *inter alia*, an LCD comprising a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.

For purposes of illustration, the embodiment of claim 1 will be discussed hereafter with reference to the embodiment depicted in FIG. 3 and the descriptions in Applicants' specification as cited below. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, FIG. 3 shows a pixel circuit for configuring an LCD panel of a low power LCD, the pixel circuit including, *inter alia*, a pixel switch N1, powers VD1 and GND, an LC unit 200 and a memory cell unit 100. The memory cell unit 100 receives first and second control signals from a first control signal line 22 and a second control signal line 23. Further, by way of example, referring to FIG. 3, when the first control signal is in a low state and the second control signal is in a high state, operation mode image signals output by a third electrode 140 of the pixel switch N1 are sent to the LC unit 200. See ¶ 27. In addition, when the first control signal is in the high state, the second control signal repeats the low state and the high state according to characteristics of the LCD panel. See ¶ 27. Accordingly, the memory cell unit 100 transmits either a

still mode image signal output by the third electrode 140 or its inverting signal to the LC unit 200. See ¶ 27.

B. Embodiments Of Claims 5 and 16

Claim 5 recites, *inter alia*, a low power LCD comprising a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel; and a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting signal.

Claim 16 recites, *inter alia*, an LCD comprising a power unit for supplying a first power, a second power and a third power to pixels; and a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage.

For purposes of illustration, the embodiments of claims 5 and 16 will be discussed hereafter with reference to the embodiment depicted in FIG. 4 and the descriptions in Applicants' specification as cited below. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, FIG. 4 shows a pixel circuit for configuring an LCD panel of a low power LCD, the pixel circuit including a pixel switch N1, powers VD1, VD2 and GND, an LC unit 200, a memory cell unit 300 and a level shift unit 400. Further, by way of example, referring to FIG. 4, the powers VD1, VD2 and GND respectively transmit a first power VD1, a second power VD2 and a third power GND to all pixels from outside the pixel area of the LCD panel. See ¶ 45. Still referring to FIG. 4, by way of example, the level shift unit 400 receives

the second control signal, lifts the high state by as much as the magnitude of the second power VD2, generates an inverting signal, and outputs the same to the memory cell unit 300. See ¶ 48. Accordingly, a voltage of an image signal transmitted to the LC unit 200 is increased to that of the second power VD2 voltage by the level shift unit 400. See ¶ 62.

C. Embodiment Of Claim 12

Claim 12 recites, *inter alia*, an LCD panel driving method comprising a memory cell unit transmitting operation mode image signals output by a pixel switch to an LC and displaying the same when the first control signal is in a low state and the second control signal is in a high state; and transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the LC as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in the high state.

For purposes of illustration, the embodiment of claim 12 will be discussed hereafter with reference to the embodiments depicted in FIGS. 3-5 and the descriptions in Applicants' specification as cited below. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, FIG. 5 shows a method for providing a first control signal to a pixel circuit configuring an LCD panel of a low power LCD driven as shown in FIGS. 3 and 4. Further, by way of example, referring to FIG. 5, when the first control signal is sequentially delayed using buffer circuits 500 and 600 and is provided to each pixel area, the first control signal becomes high and the second control signal becomes low. See ¶ 69. In addition, referring to FIG. 5,

by way of example, the second control signal is sequentially delayed by the buffer circuits 500 and 600 and is supplied to each pixel area. See ¶ 70.

Referring, by way of example, back to FIG. 3, in the normal operation mode, when the second control signal is in the high state and the first control signal is in the low state, the operation mode image signals transmitted to the third electrode 140 are transmitted to the LC unit 200 to implement moving pictures in full color. See ¶ 71. Still referring to FIG. 3, by way of example, in the still mode operation, when the first control signal becomes high and the second control signal periodically repeats high and low states according to characteristics of the LCD panel, a still pTFT P3 and an operation nTFT N2 transmit either still mode image signals transmitted to the third electrode 140 or corresponding inverting signals from drain electrodes 111 to the LC unit 200. See ¶ 71.

D. Embodiment Of Claim 18

Claim 18 recites, *inter alia*, an LCD comprising a scan driver activated to supply scanning signals for a first period and inactivated for a second period; a source driver activated to supply image signals for the first period and inactivated for the second period; and a plurality of pixels, each pixel including a memory cell storing and transmitting the image signal from a pixel switch to an LC capacitor during the first period and providing at least one of the stored image signal and an inversion signal to the LC capacitor during the second period.

For purposes of illustration, the embodiment of claim 18 will be discussed hereafter with reference to the embodiments depicted in FIGS. 2 and 4 and the descriptions in Applicants' specification as cited below. It is to be understood that the following description of the claimed embodiments and reference to the drawings are for illustrative purposes to provide some context for

the claimed embodiments, but nothing herein shall be construed as placing any limitation on the claimed embodiments.

More specifically, by way of example, FIG. 2 shows a scan driver 20 and a source driver 30. Further, by way of example, referring to FIG. 4, when a high state voltage is supplied to the scan signal line and a corresponding operation mode image signal is supplied to the source signal line, the high state voltage is supplied to a second electrode of the pixel switch N1 and image signals are transmitted to a third electrode 340 of the pixel switch N1 from the source signal line. See ¶ 61. In addition, when still mode image signals are provided, the scan driver 20 and the source driver 30 become disabled. See ¶ 63.

Referring to FIG. 4, by way of example, the memory cell unit 300 receives the first and second control signals from the first and second control signal lines 22 and 23 and receives an inverting signal of the second control signal output by the level shift unit 400. See ¶ 52. When the first control signal is in a low state and the second control signal is in a high state, operation mode image signals output by the third electrode 340 are transmitted to the LC unit 200. See ¶ 52. When the first control signal is in the high state and the second control signal repeats the low and high states according to characteristics of the LCD panel, the memory cell unit 300 transmits either a still mode image signal output by the third electrode 340 or its inverting signal to the LC unit 200. See ¶ 52.

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1, 2, 4-8 and 11-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Akiyama.

VIII. ARGUMENT

A. Rejections Under 35 U.S.C. § 103

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532 (Fed. Cir. 1993). The burden of presenting a *prima facie* case of obviousness is only satisfied by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988). A *prima facie* case of obviousness is established when the teachings of the prior art itself would appear to have suggested the claimed subject matter to one of ordinary skill in the art. In re Bell, 991 F.2d 781, 782 (Fed. Cir. 1993).

When obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000). The use of hindsight knowledge derived from the Applicants' disclosure to support an obviousness rejection under 35 U.S.C. § 103 is impermissible. See W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Thus, if the Examiner fails to establish a *prima facie* case, the rejection is improper and must be overturned. In re Rijckaert, 9 F.3d at 1532 (citing In re Fine, 837 F.2d at 1074).

Appellants respectfully submit that claims 1, 2, 4-8 and 11-18 rejected under 35 U.S.C. § 103(a) are patentable over Akiyama. For the reasons set forth below, Appellants respectfully request that the claim rejections under 35 U.S.C. § 103 be reversed.

1. Rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Akiyama

a. *Claim 1 is patentable over Akiyama because the Examiner used improper hindsight reasoning to conclude that it would have been obvious to modify Akiyama to make the memory cell unit claimed therein*

Claim 1 recites, *inter alia*, a "liquid crystal display (LCD), comprising: ... a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit."

With regard to the rejection of claim 1, in the Final Action, the Examiner indicated that Akiyama "fails to expressly teach [a] memory cell unit for receiving the first control signal and the second control signal from the control signal line unit." However, the Examiner noted that "Vref and Vcs are received by block 15 as shown in figure IA/B." Thus, according to the Examiner, it would have been obvious to one of ordinary skill in the art to utilize Akiyama to "modify the control signal line unit to provide control of memory cell 803 to obtain the apparatus Akiyama et al. modified because it would accommodate driving of still image and moving image signals, and facilitate reduction of power of LCD driver."

First, it is unclear from the Final Action how the Examiner intended to modify the structures shown in FIGS. 1A and 8 of Akiyama. Thus, the following discussion will be based on the assumption that the Examiner intended to indicate that since the block 15 receives the signals Vref and VCs2 it would have been obvious to use these signals as control signals for the memory 803.

In FIG. 1A of Akiyama, the signal Vref is provided from a reference voltage line 10 to a comparator 3 and the signal VCs2 is provided from a storage capacitor line 11 to the comparator

3. See column 10, lines 13 and 14 and column 9, lines 61 and 62. The comparator 3 compares the received signals and when one of the signals is higher than the other, the comparator 3 outputs a high level voltage. See column 10, lines 17-20. As can be gleaned, the signals Vref and VCs2 are not control signals, nor are they provided from a control signal line unit. Instead, Vref is a reference voltage such as a common voltage supplied to a plurality of pixels (see, e.g., column 10, lines 14-16) and VCs2 is a voltage corresponding to a data signal stored in a storage capacitor 2 and held in a storage capacitor 14 (see, e.g., column 10, lines 6-9).

Thus, contrary to the Examiner's assertions, since the signals Vref and VCs2 are not control signals, one of ordinary skill in the art would not use them to control the memory 803. Further, even assuming arguendo, that the signals Vref and VCs2 are control signals, there is no suggestion or motivation in Akiyama to modify Akiyama and use the signals Vref and VCs2 to control the memory 803 and make the memory cell unit as recited in claim 1. Accordingly, Appellants maintain that the Examiner improperly relied on hindsight knowledge gained from Applicants' disclosure to conclude that one of ordinary skill in the art would use the signals Vref and VCs2 to control the memory 803.

Therefore, Appellants respectfully submit that the embodiment of the invention as defined in claim 1 is patentable and nonobvious over Akiyama. In addition, for at least the reason that claims 2 and 4 depend from claim 1, claims 2 and 4 are also submitted to be patentably distinct over the cited reference.

As such, Appellants request that the Board reverse the Examiner's rejection of claims 1, 2 and 4 under 35 U.S.C. §103(a).

2. Rejection of claim 5 under 35 U.S.C. §103(a) as being unpatentable over Akiyama

Claim 5 recites, *inter alia*, a "low power liquid crystal display (LCD), comprising: ... a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel; and a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting signal".

a. *Claim 5 is patentable over Akiyama because Akiyama does not disclose the level shift unit claimed therein*

With regard to the rejection of claim 5, in the Final Action, the Examiner indicated that the claimed level shift unit is shown by an "inverting circuit 103" in FIG. 6 of Akiyama. FIG. 6 of Akiyama shows the inverting circuit 103 including an analog buffer 104, a polarity inverter 105 and analog switches 106a and b. The inverting circuit 103 receives a data signal sampled by a transistor 101 and stored in a capacitor 102, inverts the polarity of the data signal and supplies the inverted data signal to a pixel electrode 114. See column 15, lines 37-41. The inverting circuit 103 does not receive a second control signal, lift a high state by as much as a second power, generate an inverting signal, and output the inverting signal as recited in claim 5.

For example, as shown in FIG. 6, the data signal is not a control signal transmitted from a control signal line. Instead, the data signal is received from a data signal line 109. In addition, the Examiner did not indicate how the inverting circuit 103 lifts the high state by as much as the second power. The Examiner merely indicated that "the second power corresponds to that of the waveshaper 4 of figure 1B and this corresponds to the claimed 'lifting the high state by as much as the second power'." Although it is unclear from the Examiner's statement how the second power corresponds to that of the waveform shaper 4, even assuming arguendo, that the inverter

circuit 103 uses the waveform shaper 4, the waveform shaper 4 is merely used to invert the level of an output voltage of the comparator 3. See column 10, lines 24-26. The waveform shaper 4 is not used to lift a level of the output voltage much less lift a high state of the voltage by as much as a second power. Moreover, there is no suggestion or motivation in Akiyama to combine the waveform shaper 4 and the inverting circuit 103. Thus, the level shift unit of claim 5 is not taught by Akiyama.

b. *Claim 5 is patentable over Akiyama because the Examiner used improper hindsight reasoning to conclude that it would have been obvious to modify Akiyama to make the power supply unit claimed therein*

In furthering the rejection of claim 5, the Examiner indicated that Akiyama does not "teach a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of an LCD panel." However, the Examiner noted that "figure IA indicates each pixel comprises a comparator and waveform shaper 4 [and that] power of driver circuit can be turned off [and that an] opposite electrode driving circuit 904 providing voltage Vcom shown in figure 9 and Vcom corresponds to the claimed third power". Thus, according to the Examiner, it would have been obvious to one of ordinary skill in the art to utilize the apparatus of Akiyama to "provide a power unit for supplying a first power and a second power in order to energize the comparator and wave shaper for driving the LCD with AC voltage in order to reduce power consumption."

In FIG. 1A of Akiyama, a pixel of an LCD device includes the comparator 3 and the waveform shaper 4. Neither of these devices is shown having a first or second power supplied from outside of a pixel area of an LCD panel. For example, a power is not shown being provided

to the comparator 3 or the waveform shaper 4. Further, although Akiyama indicates that peripheral driving circuits such as the scanning line driver and the signal line driver can be stopped when their power is turned off (see, e.g., column 12, lines 30-32), because the comparator 3 and the waveform shaper 4 are located in the pixel area and are therefore not peripheral devices, this section of Akiyama does not apply thereto. Thus, one of ordinary skill in the art would not be motivated to modify Akiyama to make the power unit as recited in claim 5. Accordingly, Appellants maintain that the Examiner improperly relied on hindsight knowledge gained from Applicants' disclosure to conclude that one of ordinary skill in the art would modify the teachings of Akiyama to make the power unit as recited therein.

Therefore, Appellants respectfully submit that the embodiment of the invention as defined in claim 5 is patentable over and nonobvious in view of Akiyama. In addition, for at least the reason that claims 6-8, 11, 14 and 15 depend from claim 5, claims 6-8, 11, 14 and 15 are also submitted to be patentably distinct over the cited reference.

As such, Appellants request that the Board reverse the Examiner's rejection of claims 5-8, 11, 14 and 15 under 35 U.S.C. §103(a).

3. Rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over Akiyama

Claim 12 recites, an LCD panel driving method for "a pixel switch that receives scanning signals and image signals from scanning signal lines and source signal lines to output the image signals to a memory cell unit that is operated by first and second control signals or stops the image signals to display the same," comprising:

> the memory cell unit transmitting operation mode image signals output by the pixel switch to liquid crystal and displaying the same when the first control signal is in low state and the second

control signal is in high state; and

transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state.

a. *Claim 12 is patentable over Akiyama because Akiyama does not disclose the memory cell unit claimed therein*

With regard to the rejection of claim 12, in the Final Action, the Examiner indicated that a memory 803 in FIG. 8 of Akiyama corresponds to the claimed memory cell unit. FIG. 8 of Akiyama includes the memory 803 and an LC driving circuit 804 disposed downstream of transistors 801 and 802. As shown in FIG. 8, when both transistors 801 and 802 are turned on at the same time, a data signal supplied to a signal line 806 can be sampled to a pixel. See column 17, lines 24-26. In other words, the supplied data can be written to any pixel of the display screen. Although the memory 803 transmits a data signal to be displayed, the data signal is not transmitted when the first control signal is in a low state and the second control signal is in a high state. Instead, the data signal is transmitted when both transistors 801 and 802 are turned on at the same time and in response to scanning signals supplied from gate lines 807 and 808. See column 17, lines 29-31. In other words, the transistors 801 and 802 are turned on and off by data scanning signals, not control signals. Thus, the memory cell unit of claim 12 is not taught by Akiyama.

b. *Claim 12 is patentable over Akiyama because the Examiner used improper hindsight reasoning to conclude that it would have been obvious to modify Akiyama to transmit signals from the memory cell unit as claimed therein*

In furthering the rejection of claim 12, the Examiner indicated that Akiyama "fails to expressly teach when the first control signal is in low state and the second control signal is in high

state." However, the Examiner indicated that "[o]ne skilled in the art would know how to selectively control a memory cell in order to read/write" and that Akiyama "teaches different image signals from still picture and moving picture (figure 9)." Thus, the Examiner posited, that it would have been obvious to one of ordinary skill in the art to utilize the method of Akiyama to "provide selective control of the memory [803] in order to accommodate driving the LCD with [a] plurality of image signal types (still picture and moving picture)." In addition, the Examiner indicated that a periodically repeating control signal [e.g., the second control signal] is shown in FIGS. 11 C and D of Akiyama.

FIGS. 11C and D of Akiyama illustrate pixels that have the capability of generating an AC voltage corresponding to sampled data. See column 9, lines 9-13. For example, in FIGS. 11C and D, signals Vref or Vcom may periodically alternate. However, these signals are not used as control signals for causing a still mode image signal or its inverting signal to be output to an LC layer 5. Instead, they are used as constant supply voltages. See column 19, lines 31-34.

In addition, even if the signals Vref or Vcom were used as control signals, there is no suggestion or motivation in Akiyama to use either one as a control signal for causing a still mode image signal or its inverting signal to be output. For example, there is no suggestion or motivation in Akiyama to provide first and second control signals to the memory 803 for at least the reasons discussed above for claim 1. In addition, Akiyama does not teach or suggest providing an inverting signal to the memory 803 for at least the reasons discussed above for claim 5. Accordingly, Appellants maintain that the Examiner improperly relied on hindsight knowledge gained from Applicants' disclosure to conclude that one of ordinary skill in the art would modify the teachings of Akiyama to transmit signals from the memory cell unit as recited in claim 12.

Therefore, Appellants respectfully submit that the embodiment of the invention as defined in claim 12 is patentable over and nonobvious in view of Akiyama. In addition, for at least the reason that claim 13 depends from claim 12, claim 13 is also submitted to be patentably distinct over the cited reference.

As such, Appellants request that the Board reverse the Examiner's rejection of claims 12 and 13 under 35 U.S.C. §103(a).

4. Rejection of claim 16 under 35 U.S.C. §103(a) as being unpatentable over Akiyama

a. *Claim 16 is patentable over Akiyama for at least the reasons discussed above for claim 5 and because Akiyama does not disclose a level shift unit for increasing a voltage*

Claim 16 recites, *inter alia*, a "power unit for supplying a first power, a second power and a third power to pixels; and a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage".

With regard to the rejection of claim 16, in the Final Action, the Examiner indicated that Akiyama does not teach "a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage." However, the Examiner noted that Akiyama discloses "an inverting circuit (103) including a polarity inverter (105) [and] that the output voltage V2 of an analog buffer 104 or an output voltage -V2 of the polarity inverter 105 are selected by the analog switches 106a and 106b and the selected voltage is supplied to the pixel electrode 114." Thus, according to the Examiner, it would have been obvious to one of ordinary skill in the art "to utilize the selection of voltage with respect to [a] pixel electrode for the purpose of setting the amount of voltage needed."

As stated and argued above with respect to claim 5, Appellants respectfully submit that Akiyama fails to teach or suggest a power unit for supplying a first power, a second power and a third power to pixels. In addition, Akiyama fails to teach or disclose the level shift unit. Further, Akiyama does not disclose the feature of increasing a voltage as recited in claim 16. For example, the inverting circuit 103 merely inverts the polarity of a data signal and supplies the data signal or an inverted version of the data signal to a pixel electrode 114. See column 15, lines 49-65. The inverting circuit 103 does not increase a voltage of the data signal. Instead, the inverting circuit 103 either maintains a voltage of the data signal or reverses the polarity of the data signal.

Therefore, Appellants respectfully submit that the embodiment of the invention as defined in claim 16 is patentable over and nonobvious in view of Akiyama. In addition, for at least the reason that claim 17 depends from claim 16, claim 17 is also submitted to be patentably distinct over the cited reference.

As such, Appellants request that the Board reverse the Examiner's rejection of claims 16 and 17 under 35 U.S.C. §103(a).

5. Rejection of claim 18 under 35 U.S.C. §103(a) as being unpatentable over Akiyama

Claim 18 recites, a liquid crystal display comprising:

> a scan driver activated to supply scanning signals for a first period and inactivated for a second period;
>
> a source driver activated to supply image signals for the first period and inactivated for the second period; and
>
> a plurality of pixels, each pixel including a liquid crystal capacitor displaying an image, a pixel switch for transmitting the image signals in response to the scanning signal, and a memory cell storing and transmitting the image signal from the pixel switch to the liquid crystal capacitor during the first period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the second period.

a. *Claim 18 is patentable over Akiyama because Akiyama does not disclose the memory cell claimed therein*

With regard to the rejection of claim 18, in the Final Action, the Examiner indicated that the claimed memory cell is shown by a "memory 202" of FIG. 7 of Akiyama. In FIG. 7, Akiyama shows a pixel of an LCD device including the memory 202 coupled between and sampling circuit 201 and a DAC 203. As can be gleaned, the memory 202 does not provide at least one of a stored image signal and an inversion signal to an LC capacitor during a second period in which, for example, a signal line driving circuit 902 (of FIG. 9) and a gate line driving circuit 903 (of FIG. 9) are inactivated. Instead, the memory 202 merely provides stored digital data to the DAC 203. See, column 16, lines 48-67. The memory 202 does not provide an inversion signal to an LC capacitor as it does not receive the inversion signal from the inverting circuit 103. Thus, the memory cell of claim 18 is not taught by Akiyama.

b. *Claim 18 is patentable over Akiyama because the Examiner used improper hindsight reasoning to conclude that it would have been obvious to modify Akiyama to transmit signals from the memory cell as claimed therein*

In furthering the rejection of claim 18, the Examiner indicated that Akiyama does not teach "a source and scan driver being inactivated for a second period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the second period." To cure this deficiency in Akiyama, the Examiner indicated that it would have been obvious to one of ordinary skill in the art to "utilize Akiyama's inverting circuit 103 ... fro [sic] the purposed of inverting the polarity of a given signal in a desired fashion" and to "utilize Akiyama's pixel electrode (114) as configured with analog switches

(106a, 106b) along with Akiyama's teaching of relevant signals being stopped fro [sic] the purpose of achieving inactivation with respect to drivers in a given period."

Although Akiyama discloses the signal line driving circuit 902 and the gate line driving circuit 903 that may be active and during different periods, Akiyama does not disclose the claimed memory cell. For example, as discussed above, the memory 202 does not provide at least one of the stored image signal and an inversion signal to an LC capacitor during a second period in which the signal line driving circuit 902 and a gate line driving circuit 903 are inactivated. Further, there is no suggestion or motivation in Akiyama to combine the memory 202 and the inverting circuit 103. Accordingly, Appellants maintain that the Examiner improperly relied on hindsight knowledge gained from Applicants' disclosure to conclude that one of ordinary skill in the art would modify the teachings of Akiyama to transmit signals from the memory cell as recited in claim 18.

Therefore, Appellants respectfully submit that the embodiment of the invention as defined in claim 18 is patentable over and nonobvious in view of Akiyama.

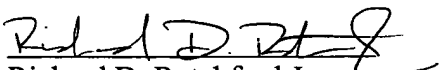
As such, Appellants request that the Board reverse the Examiner's rejection of claim 18 under 35 U.S.C. §103(a).

B. CONCLUSION

Accordingly, for at least the reasons set forth above, claims 1, 2, 4-8 and 11-18 are patentable and nonobvious over Akiyama.

Therefore, it is respectfully requested that the Board reverse all claim rejections under 35 U.S.C. § 103(a).

Respectfully submitted,



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CLAIMS APPENDIX

1. A liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for selectively providing the image signals to a third electrode from a first electrode connected to the source signal line depending on voltage state of a second electrode connected to the scan signal line;

a power unit for respectively supplying first power and second power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit including a first control signal line for transmitting a first control signal to all pixels from outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from the outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting according to voltage difference between the image signals and the second power; and

a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.

2. The liquid crystal display (LCD) of claim 1, wherein the third electrode of the pixel switch outputs an operation mode image signal to the liquid crystal unit, when the first control signal is in low state and the second control signal is in high state.

3. The liquid crystal display (LCD) of claim 1, wherein the memory cell unit further comprises:

a first inverter circuit including a nTFT and a pTFT, a drain electrode of the nTFT is connected to the pTFT, and gate electrodes of the first inverter circuit are connected to the third electrode of the pixel switch;

a second inverter circuit including a nTFT and a pTFT, drain electrodes of the second inverter circuit are connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit are connected to the drain electrodes of the first inverter circuit;

a push nTFT including a drain electrode connected to the first power, a source electrode connected to a source electrode of the pTFTs of the first and second inverter circuits and a gate electrode of the push nTFT connected to the first control signal line;

a pull nTFT including a source electrode connected to the second power, a drain electrode connected to source electrodes of the nTFTs of the first and second inverter circuits and a gate electrode of the pull nTFT connected to the first control signal line;

an operation nTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT are connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still pTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the still pTFT connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

4. The liquid crystal display (LCD) of claim 1, wherein the pixel area of the LCD panel is divided into at least two portions and the control signal line transmits control signals sequentially delayed by a buffer circuit to corresponding pixel areas.

5. A low power liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for selectively outputting the image signals to a third electrode from a first electrode connected to the source signal line depending on voltage state of a second electrode connected to the scan signal line;

a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit including a first control signal line for transmitting a first control signal to all pixels from the outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting light according to a difference between the image signals and the third power; and

a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting signal.

6. The liquid crystal display (LCD) of claim 5, further comprising a memory cell unit.

7. The liquid crystal display (LCD) of claim 6, wherein the memory cell unit receives the first and second control signals from the control signal line unit and receiving the inverting signal of the second control signal output by the level shift unit.

8. The liquid crystal display (LCD) of claim 7, wherein an operation mode image signal is selectively output by a third electrode of the pixel switch and the operation mode signal

is selectively transmitted to the liquid crystal unit.

9. The liquid crystal display (LCD) of claim 7, wherein the memory cell unit comprises:

a first inverter circuit including a nTFT and a pTFT, a drain electrode of the nTFT connected to the pTFT, and gate electrodes of the first inverter circuit are connected to the third electrode of the pixel switch;

a second inverter circuit including a nTFT and a pTFT, drain electrodes of the nTFT and pTFT connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit nTFT and pTFT are connected to the drain electrodes of the first inverter circuit;

a push nTFT including a drain electrode connected to the first power, a source electrode connected to source electrodes of the pTFTs of the first and second inverter circuits, and a gate electrode connected to the first control signal line;

a pull nTFT including a source electrode connected to the third power, a drain electrode connected to source electrodes of the nTFTs of the first and second inverter circuits and the second inverter circuit, and a gate electrode connected to the first control signal line;

an operation nTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still nTFT having a gate electrode connected to receive an inverting signal of the second control signal output by the level shift unit, and source and drain electrodes of the still nTFT connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

10. The liquid crystal display (LCD) of claim 5, wherein the level shift unit

comprises:

a third inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT is connected to that of the pTFT of the third inverter circuit, gate electrodes are connected to the second control signal line, a source electrode of the pTFT is connected to the second power, and a source electrode of the nTFT is connected to the third power; and

a level-up pTFT having a gate electrode connected to a drain electrode of the third inverter circuit, a source electrode of the level-up pTFT is connected to the second power, and a drain electrode of the level-up pTFT is connected to the second control signal line.

11. The liquid crystal display (LCD) of claim 5, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions.

12. A liquid crystal display (LCD) panel driving method for a pixel switch that receives scanning signals and image signals from scanning signal lines and source signal lines to output the image signals to a memory cell unit that is operated by first and second control signals or stops the image signals to display the same, an LCD driving method comprising:

the memory cell unit transmitting operation mode image signals output by the pixel switch to liquid crystal and displaying the same when the first control signal is in low state and the second control signal is in high state; and

transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state.

13. The method of claim 12, wherein the pixel area of the LCD panel is divided into at least two portions in either a horizontal or vertical direction and respective control signals are transmitted and-sequentially delayed by a buffer circuit according to a corresponding pixel area.

14. The liquid crystal display of (LCD) claim 7, wherein the third electrode of the pixel switch selectively outputs a still mode image signal.

15. The liquid crystal display of (LCD) claim 7, wherein the second control signal periodically repeats the low and high states according to characteristics of the LCD panel to selectively transmit an inverting signal to the liquid crystal unit.

16. A liquid crystal display (LCD), comprising:

a scan signal line;

a source signal line;

a pixel switch for selectively outputting image signals;

a power unit for supplying a first power, a second power and a third power to pixels;

a first control signal line for transmitting a first control signal to the pixels;

a second control signal line for transmitting a second control signal to the pixels; and

a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage.

17. A liquid crystal display (LCD) of claim 16, wherein the level shift unit outputs the generated inverting signal.

18. A liquid crystal display, comprising:

a scan driver activated to supply scanning signals for a first period and inactivated for a second period;

a source driver activated to supply image signals for the first period and inactivated for the second period; and

a plurality of pixels, each pixel including a liquid crystal capacitor displaying an image, a pixel switch for transmitting the image signals in response to the scanning signal, and a memory cell storing and transmitting the image signal from the pixel switch to the liquid crystal capacitor during the first period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the second period.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132 or any other evidence entered by the Examiner and relied upon by Appellant in this Appeal.

RELATED PROCEEDINGS APPENDIX

None.